Short Course

Analog-to-Digital Converters

This Short Course is intended to provide both entry-level and experienced engineers with practical approaches to the design of analog-to-digital converters. The course provides an overall perspective on the technology considerations, circuit-design issues, and detailed design strategies, for circuit building blocks in analog-to-digital converters. Topics covered address the challenges faced by analog designers in current and future technologies, with an emphasis on detailed circuit-design approaches, and methodologies for deep-submicron integration.

OUTLINE

Fundamental Limits and Practical Design Issues in A/D Converters

In this presentation, fundamental limitations of ADCs associated with noise, clock jitter, power consumption, and conversion rate, are discussed. Figures-of-merit (FoM) based on these fundamental limits will be compared in various ADC topologies including flash, pipeline, successive-approximation, and $\Delta\Sigma$ converters. Design strategies for improving FoMs in practical ADCs will also be discussed. Finally, practical design issues, such as component mismatch, finite-gain effects, charge injection, and substrate noise with techniques for reducing its effects, will be described.

Instructor: Hae-Seung Lee received his Ph.D. from the University of California, Berkeley, in 1984, where he pioneered self-calibration techniques for A/D converters. In 1984, he joined the faculty at the Massachusetts Institute of Technology, Cambridge, MA, where he is now Professor and Director of the Center for Integrated Circuits and Systems. Since 1985, he has acted as a consultant to Analog Devices, Lincoln Laboratories, and Cypress Semiconductor. He has authored or co-authored more than 100 journal and conference papers. He is a Fellow of the IEEE.

Pipelined A/D Converters

As CMOS processes scale down, ADC designers benefit greatly from both device speed and lithographic accuracy: Device speed contributes directly to the prevailing trend toward oversampling techniques in high-resolution ADC designs. On the other hand, finer-line feature size offers better component matching for a fixed device size, and Nyquist-rate pipelined techniques still provide power- and area-efficient solutions for high-speed medium-resolution applications. Correspondingly, advanced pipelined ADC techniques have been further developed to enhance resolution. This presentation begins by identifying the fundamental limits in achieving accuracy and speed with basic pipelining techniques. It will then focus on design issues related to high speed and high resolution.

Instructor: Bang-Sup Song received his Ph.D. from the University of California, Berkeley, in 1983. He was with AT&T Bell Laboratories, Murray Hill, and the ECE Department, University of Illinois, Urbana-Champaign, before he joined the ECE Department, University of California, San Diego, in 1999, where he is endowed as the Charles Lee Powell Chair Professor in Wireless Communication. His current interest is in CMOS analog circuits including data converters, wireless transceivers, TV tuners, frequency synthesizers, image-rejection techniques, active filters, and timing recovery. His research has been focused on improving analog-circuit performance using digital aids. He is an IEEE Fellow.

$\Delta\Sigma$ ADCs

Delta-sigma ADCs are the preferred architecture when dynamic-range requirements exceed 13 bits or so. This presentation will explore the most important properties of delta-sigma ADCs, including inherent linearity, and (for continuous-time systems) inherent anti-aliasing. These properties are illustrated in the context of the simplest delta-sigma ADC, the first-order modulator, and then generalized to second- and higher-order modulators. Then, bandpass modulation, quadrature modulation, cascade modulation, and mismatch-shaping, are introduced, and shown to fit into the same basic framework, namely that of high-gain linear feedback around a nonlinear element. Each of these delta-sigma variants is illustrated with examples constructed using the Delta-Sigma Toolbox.

Instructor: Richard Schreier received his Ph.D. from the University of Toronto, in 1991. From 1985 to 1987, he worked at Bell-Northern Research in Ottawa, Canada, and, from 1991 to 1997, he was an Assistant/Associate Professor at Oregon State University in Corvallis. Since 1997, he has been working for Analog Devices, Inc. in Wilmington, Massachusetts. In 2002, he received the ISSCC outstanding-paper award for a paper describing a 50mW bandpass delta-sigma ADC with 90dB of dynamic range, and 300kHz of bandwidth. He co-edited an IEEE Press book (with S.R. Norsworthy and G.C. Temes), published in 1997. His second book (with G.C. Temes) on delta-sigma modulation was published in 2004. He is also the author of the freeware Delta-Sigma Toolbox for MATLAB.

Sub-1V Analog-to-Digital Converters

The analog-to-digital converter is an important analog-interface circuit-block. However, it is becoming a critical bottleneck in mixed-signal IC systems, as CMOS-transistor dimensions shrink in state-of-the-art technology. This is due to the fact that transistors of smaller dimensions can tolerate only a proportionally smaller voltage stress. This presentation will review the low-voltage problem, summarize some of the well-known solutions currently in use (and their associated problems), and introduce recently-developed circuit techniques. A few IC-implementation results for both oversampling and Nyquist analog-to-digital converters which operate below 1V will be presented as possible design solutions for future low-voltage submicron CMOS processes.

Instructor: Un-Ku Moon received his B.S. from the University of Washington, his M.Eng. from Cornell University, and his Ph.D. from the University of Illinois, Urbana-Champaign, all in electrical engineering. He has been with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, since 1998, where he is currently an Associate Professor. Before joining Oregon State University, he was with Bell Laboratories from 1994 to 1998, as well as from 1988 to 1989. His research interests include highly-linear and tunable continuous-time filters, telecommunication circuits including timing-recovery and data-converters, and ultra-low-voltage analog circuits.